low concentration impurity layer 1 having an identical conductivity (col. 4, line 3). Applicants respectfully disagree.

Claim 1 recites, *inter-alia*, "A dielectrically separated wafer having a plurality of dielectrically separated monocrystalline silicon islands mutually defined by a dielectrically separating oxide film on a surface of the wafer..." Claim 5 recites, *inter-alia*, "A diellectrically separated wafer having a plurality of dielectrically separated monocrystalline silicon islands insulated by a dielectrically separating oxide film on the wafer surface, the diellectrically separated wafer comprises a surface between one diellectrically separated silicon island and another neighboring dielectrically separated silicon island formed so as to be flat." The surface of the dielectrically separated silicon wafer has a flatness which is less than 0.2 μm. Whereas the grinding method of Ohta et al. cannot prevent the formation of an indentation 16a and a projection 16b having a step of approximately 0.3 μm or larger in a border of polysilicon layer 16 of Ohta et al. The present invention eliminates this problem by having a surface flatness less than 0.2 μm.

Consequently, Ohta et al. does not disclose, teach or suggest the subject matter recited in claim 1 and claim 5.

Therefore, the Applicants respectfully submit that claim 1 and claim 5 are patentable and request that the §102 rejection of claims 1 and 5 be withdrawn.

Claim 6 was rejected under 35 U.S.C. 102(b), or in the alternative, under 35 U.S.C. 103(a) as obvious over Ohta et al. Applicants traverse this rejection for at least the following reasons.

The Office Action contends that Ohta et al. teach the device of claim 5. The Office Action admits however that Ohta et al. did not expressly disclose that a flatness on the surface of the dielectrically separated islands is less than 0.2 μm when measured by a stylus-profilometer. The Examiner contends that this limitation is considered taught or obvious over Ohta et al. because the grinding will inherently create a surface having no difference between the maximum and minimum values of flatness and that it is considered within one of skill in the art to minimize any surface roughness as motivated by the relationship between the surface roughness and complications in processing. Applicants respectfully disagree.

The grinding method of Ohta et al. cannot prevent the occurrence of an indentation 16a and a projection 16b having a step of approximately 0.3 μm or greater in a border of

polysilicon layers 16. As stated above, the present invention eliminates this problem by having a surface flatness less than 0.2 μm.

Ohta et al. merely intends to prevent a convex warpage toward a polycrystalline silicon in a semiconductor wafer which causes deterioration in a product yield for semiconductor integrated circuit. For such a purpose, Ohta et al. discloses that an irreversibly thermally shrinkable film is formed on a rear surface of a single crystal silicon substrate (lines 44 to 46 column 2 in Ohta et al.). By doing so, it is possible to prevent the occurrence of warpage in the semiconductor wafer because a shrinking force in the reversibly thermally shrinkable film convexly toward the polycrystalline silicon layer and a warping force in a deposited polycrystalline silicon layer concavely toward the polycrystalline silicon are offset from each other (lines 11 to 27 in Column 3 of Ohta et al.).

Moreover, Ohta et al. teaches that it is sufficient for a surface of a polycrystalline silicon layer 8 to be finished flat and smooth (in lines 58 of column 5 to line 9 of column 6). However, with regard to limitations in the grinding operation, Ohta et al. merely teaches that the thickness of the polycrystalline silicon layer 8 to be removed by grinding operation is desired to be approximately in the range of 30 to 60 μm such that the warpage of the substrate will be kept in the range of 0 to 80 μm.

In contrast, the present invention provides the manufacture of a dielectrically separated wafer without causing a defect pattern due to the adhesion of a resist, circuit connection, bad resolution, and removal of a mask only under conditions that a step in the indentation 16a and a projection 16b are approximately 0.2μm or smaller. Moreover, in order to achieve such a preferable dimension in the steps in the indentation 16a and the projection 16b, preferable conditions which are based on factors such as amount of polishing L1 (μm) and thickness of dielectrically separating oxide film (μm) are finally found by testing various conditions shown in TABLES 1 to 4 of the present application. The accuracy such as ± 0.2 μm achieved in the present invention differs from the limitations 30 to 60 μm taught by Ohta et al.

Consequently, for at least the above reasons, Applicants submit that Ohta et al. does not disclose, teach or suggest the subject matter recited in claim 6.

Therefore, Applicants respectfully submit that claim 6 is patentable and respectfully request that the §102 and §103 rejections of claim 6 be withdrawn.

Claim 3 was rejected under 35 U.S.C. 102(b) over Katayama and claim 9 was rejected under 35 U.S.C. 102(b), or in the alternative, under 35 U.S.C. 103(a) as obvious over Katayama et al. Applicants traverse these rejections of the at least the following reasons.

The Office Action contends that Katayam et al. teaches the device recited in claim 3. The Office Action, however, admits that Katayama et al. does not disclose that a flatnes on the surface of the dielectrically separated islands is less than 0.2μm when measured by a stylus-profilometer. The Office Action contends that this limitation is considered either taught or in the alternative obvious over Katayama et al. since Katayama et al. teaches that both surfaces 2a and 2b are polished flatwise to form islands and as such it is considered inherent that the polishing will create a surface having no difference between minimum and maximum values of flatness. The Office Action thus contends that it is obvious to one of ordinary skill in the art to minimize any surface roughness as motivated by the the relationship between surface roughness and complications of processing subsequent layers. Applicants respectfully disagree.

Katayama et al. relates to a different technical area than the present invention. Indeed, Katayama et al. relates to a method for forming a polysilicon layer without causing a warpage therein. In Katayama et al., a first polysilicon layer is formed on the separation oxide film according to a low-temperature and low-pressure chemical vapor growth method, and a second polycrystalline silicon layer is formed according to a high-temperature and normal-pressure chemical vapor growth method. Therefore, Katayama does not disclose, teach or suggest a surface flatness as an absolute roughness between a maximum height and a minimum height is less than 0.2 μm.

Consequently, for at least for the above reasons, Katayama et al. does not disclose teach or suggest the subject matter recited in claim 9.

Therefore, Applicants respectfully submit that claim 9 is patentable and respectfully request that the §102 and §103 rejections of claim 9 be withdrawn.

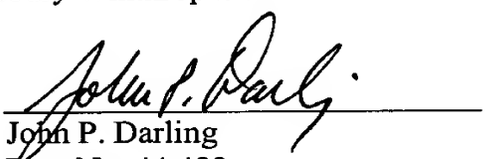
CONCLUSION

In view of the foregoing, the claims are now in form for allowance, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, he is kindly requested to contact the undersigned at the telephone number listed below.

All objections and rejections having been addressed, it is respectfully submitted that the present application is in a condition for allowance and a Notice to that effect is earnestly solicited.

Respectfully submitted,

Pillsbury Winthrop LLP

By: 

John P. Darling
Reg. No. 44,482
Tel. No.: (703) 905-2045
Fax No.: (703) 905-2500

JPD/KG

1600 Tysons Boulevard
McLean, Virginia 22102